PATENT ABSTRACTS OF JAPAN

(11)Publication number : 10-125725

(43)Date of publication of application : 15.05.1998

(51)Int.Cl. H01L 21/60

(21)Application number : 08-276053

(22)Date of filing : 18.10.1996

(71)Applicant : MITSUBISHI ELECTRIC CORP

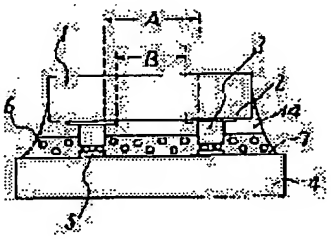
(72)Inventor : HAMAGUCHI TSUNEO
TSURUTA AKIZO
TOSHIDA KENJI
ISHIZAKI MITSUNORI
KITAMURA YOICHI
NAGAMINE TAKAHIRO

(54) SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can prevent deterioration of insulating property of a conductive adhesive narrowly provided between fine electrodes of a semiconductor element caused by conductive particles of the adhesive, and which can connect the semiconductor element to a wiring substrate with a good productivity.

SOLUTION: The semiconductor device includes a semiconductor element 1 having electrodes 2 and projected electrodes 3 each having a sectional area smaller than each of the electrodes 2, a wiring substrate 4 having electrodes 5 provided at positions opposed to the projected electrodes 3, and a plurality of adhesive layers provided between the element 1 and substrate 4. The plurality of adhesive layers include an adhesive-alone layer 14 not containing conductive particles 6 and arranged on the side of the element 1, and an anisotropy conductive adhesive layer 7 provided on the side of the substrate 4 for conducting the electrodes 3 and the electrodes 5 on the substrate and opposed thereto.



LEGAL STATUS

[Date of request for examination] 05.09.2001

[Date of sending the examiner's decision of rejection] 02.12.2003

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by to have the layer of the anisotropy electric-conduction adhesives which it is formed [adhesives] between the semiconductor device which has the projection electrode of the cross section smaller than this electrode on an electrode, the wiring substrate which has said projection electrode and the electrode arranged in the location which counters, and said semiconductor device and said wiring substrate, and make it flow through said projection electrode and the electrode on said wiring substrate which counters this.
[Claim 2] The semiconductor device which has the projection electrode of the cross section smaller than this electrode on an electrode, The wiring substrate which has said projection electrode and the electrode arranged in the location which counters, It is the semiconductor device equipped with the two or more layers layer of adhesives formed between said semiconductor devices and said wiring substrates. Said two or more layers layer of adhesives The semiconductor device characterized by being in said layer [of the adhesives which are in said semiconductor device side and do not contain an electric conduction particle], and wiring substrate side, and consisting of layers of the anisotropy electric conduction adhesives which make it flow through said projection electrode and the electrode on said wiring substrate which counters this.
[Claim 3] A wiring substrate is a semiconductor device according to claim 1 or 2 characterized by being a glass substrate.
[Claim 4] A wiring substrate is a semiconductor device according to claim 1 or 2 characterized by carrying out the laminating of a printed circuit board and the wiring layer formed by resin material.
[Claim 5] A wiring substrate is a semiconductor device according to claim 1 or 2 characterized by being the wiring layer which consisted of resin material with flexibility.
[Claim 6] The manufacture approach of the semiconductor device characterized by to have the process which forms the projection electrode which has the cross-sectional area smaller than this electrode by the ball bonder on the electrode of a semiconductor device, the process which pastes up anisotropy electric conduction adhesives on the field in which the electrode on a wiring substrate and wiring were formed, and the process which pushes said projection electrode against the electrode of said wiring substrate through said anisotropy electric conduction adhesives.
[Claim 7] The process which forms the layer of the adhesives which do not contain an electric conduction particle in the front face of the semiconductor device which has the projection electrode of the cross section smaller than this electrode on an electrode, The process which forms the layer of anisotropy electric conduction adhesives in the field in which the electrode on a wiring substrate and wiring were formed, The manufacture approach of the semiconductor device characterized by having the process which pushes the semiconductor device in which the layer of the adhesives which do not contain said electric conduction particle was formed, and the wiring substrate with which the layer of anisotropy electric conduction adhesives was formed, and is pasted up.

[Translation done.]

* NOTICES *
JPO and NCIPI are not responsible for any
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device obtained by connecting the electrodes of a wiring substrate with a semiconductor device with anisotropy electric conduction adhesives, and its manufacture approach.
[0002]
[Description of the Prior Art] Since electronic equipment is miniaturized more, it has changed to the approach of mounting a semiconductor device in a wiring substrate with nakedness without packing, from the approach of soldering the packed semiconductor device to a wiring substrate. There is the approach of pasting up the rear face of a semiconductor device on a wiring substrate with electroconductive glue, and connecting the electrode of a semiconductor device and the electrode of a wiring substrate with a wire as an approach of mounting a semiconductor device in a wiring substrate with nakedness. This approach requires time amount for connecting many electrodes in order to connect a semiconductor device and the electrode of a wiring substrate with 1 1 wire. Moreover, in order to arrange the electrode of the wiring substrate connected around a semiconductor device, a component-side product needs to take more greatly than the area of a semiconductor device. Then, as an approach of mounting in the almost same area as a semiconductor device, the semiconductor device was turned over and the flip-chip-bonding approach which carries out direct continuation to a wiring substrate electrode was developed.
[0003] There are an approach (for example, the Nikkan Kogyo Shimbun issue, a surface mount technology, September issue 1994, 48 pages) of connecting using (1) electroconductive glue as the approach and the approach (for example, Kogyo Chosakai Publishing, June 1, 1986 issue, Sir face mounting technology, 172 pages) of connecting using (2) solder. Hereafter, it explains, referring to a drawing. Drawing 7 is the sectional view showing the configuration of the conventional semiconductor device connected using electroconductive glue. In drawing, the electrode with which the semiconductor device of the nakedness which 1 has not packed, the electrode with which 2 was formed on the semiconductor device 1, the projection electrode with which 3 was formed on the electrode 2 on this semiconductor device, and 4 were formed in the wiring substrate, and 5 was formed on the wiring substrate 4, and 21 show electroconductive glue, and 22 shows encapsulant.
[0004] The manufacture approach of the conventional semiconductor device with such structure is explained. First, the projection electrode 3 is formed on the electrode 2 of a semiconductor device 1 using plating. Next, this projection electrode 3 is pushed against the electroconductive glue layer (not shown) formed in the plate at homogeneous membrane thickness, and electroconductive glue 21 is imprinted to the projection electrode 3. Next, a semiconductor device 1 is forced on the wiring substrate 4 for a semiconductor device 1 and the wiring substrate 4 after ********** of facing each other, the projection electrode 3 of a semiconductor device 1, and the electrode 5 on the wiring substrate 4, and the projection electrode 3 and the electrode 5 on the wiring substrate 4 are contacted through electroconductive glue 21. Next, after heating on about 150-degree C conditions for several hours and stiffening electroconductive glue 21, the encapsulant 22 for protecting invasion of moisture etc. from the exterior is poured in between a semiconductor device 1 and the wiring substrate 4, and the semiconductor device shown in drawing 7 can be obtained by carrying out heat hardening.
[0005] Drawing 8 is the sectional view showing the configuration of the conventional semiconductor device in the case of connecting using solder. In drawing, the electrode with which the electrode with which 1 was formed in the semiconductor device and 2 was formed on the semiconductor device 1, the projection electrode with which 3 was formed on the electrode 2 on this semiconductor device, and 4 were formed in the wiring substrate, and 5 was formed on the wiring substrate 4, and 22 show encapsulant, and 23 shows solder. The manufacture approach of the conventional semiconductor device with such structure is explained. First, on two of the electrode formed on the semiconductor device 1, after forming the film of Cr and Cu by vacuum evaporationo etc., patterning of the resist is carried out and the projection electrode 3 of the solder of Pb-Sn is formed by plating or vacuum evaporationo. Next, the semiconductor device shown in drawing 8 can be obtained by performing the electrode 5 and alignment on the wiring substrate 4 which has supplied the eutectic solder 23 beforehand, heating a

semiconductor device 1, carrying out melting of the solder 23, joining the projection electrode 3 and an electrode 5, pouring in encapsulant 22 and carrying out heat hardening between a semiconductor device 1 and the wiring substrate 4.

[0006] Drawing 9 is the sectional view showing the configuration of the conventional semiconductor device which connects a semiconductor device and a wiring substrate with the anisotropy electric conduction adhesives indicated by JP,62-6652,B. In drawing, in the electrode with which 1 was formed in the semiconductor device and 2 was formed on the semiconductor device 1, the projection electrode with which 3 was formed on the electrode 2 on this semiconductor device, and 4, a wiring substrate and 7 show the layer of anisotropy electric conduction adhesives, and 9 shows the electric conduction lead wire on the wiring substrate 4. In addition, anisotropy electric conduction adhesives are what distributed in adhesives metal particles, the particle which ****(ed) the metal on the front face of a plastic bowl, if a pressure is applied, adhesives will be eliminated and an electric flow will be obtained.

[0007] If the layer 7 of anisotropy electric conduction adhesives is formed on the electric conduction lead wire 9 on the wiring substrate 4 and the semiconductor device 1 with the projection electrode 3 is forced, the layer 7 of the anisotropy electric conduction adhesives of the part under the projection electrode 3 will flow in the direction in which the pressure was applied. Thereby, the projection electrode 3 and the electric conduction lead 9 flow. To coincidence, a semiconductor device 1 can be fixed according to an adhesion operation of the layer 7 of anisotropy electric conduction adhesives to the wiring substrate 4, and can prevent invasion of the moisture from the outside, or dust. Moreover, since the inferior surface of tongue of a semiconductor device 1 is extensively pasted up on the wiring substrate 4 by the layer 7 of anisotropy electric conduction adhesives, adhesion area becomes large and bonding strength also becomes strong.

[0008]

[Problem(s) to be Solved by the Invention] There were the following troubles in the conventional semiconductor device shown in drawing 7 and drawing 8 .

(1) When a semiconductor device is pressed against a wiring substrate electrode for connection, electroconductive glue or the adhesives of solder contacts breadth and an adjoining electrode horizontally, short-circuit occurs, and connection of the semiconductor device of detailed inter-electrode distance cannot be performed.

(2) After connecting the projection electrode of a semiconductor device, and the electrode of a wiring substrate with electroconductive glue or solder, in order to raise dependability and to pour in encapsulant between a semiconductor device and a wiring substrate, a process lacks in productivity mostly.

[0009] Although the conventional technique shown in drawing 9 had solved these troubles once, the conductive particle of electroconductive glue existed in projection inter-electrode A, and there was a trouble that projection inter-electrode conductive particles recriminate, projection inter-electrode insulation resistance deteriorates, or the conductive channel by the electric conduction particle was made to inter-electrode [in the front face of a semiconductor device], and inter-electrode insulation deteriorated in the semiconductor device which has the detailed electrode with which an electrode spacing A becomes narrow.

[0010] insulating degradation to which this invention originates in the electric conduction particle of the electroconductive glue by which it is placed between inter-electrode also in the semiconductor device which has a detailed electrode with a narrow electrode spacing — preventing — further — a wiring substrate — fitness — it aims at offering the semiconductor device which makes connection with sufficient productivity, and its manufacture approach.

[0011]

[Means for Solving the Problem] The semiconductor device concerning this invention is formed between the semiconductor device which has the projection electrode of the cross section smaller than this electrode on an electrode, the wiring substrate which has a projection electrode and the electrode arranged in the location which counters, and a semiconductor device and a wiring substrate, and is equipped with the layer of the anisotropy electric-conduction adhesives which make it flow through a projection electrode and the electrode on said wiring substrate which counters this.

[0012] Moreover, the semiconductor device to which the semiconductor device concerning this invention has the projection electrode of the cross section smaller than this electrode on an electrode, It is the semiconductor device equipped with the two or more layers layer of adhesives formed between the wiring substrate which has a projection electrode and the electrode arranged in the location which counters, and a semiconductor device and a wiring substrate. The two or more layers layer of adhesives is in a layer [of the adhesives which are in a

semiconductor device side and do not contain an electric conduction particle], and wiring substrate side, and consists of layers of the anisotropy electric conduction adhesives which make it flow through a projection electrode and the electrode on the wiring substrate which counters this.

[0013] Moreover, the wiring substrate of the semiconductor device concerning this invention is characterized by being a glass substrate. Moreover, the wiring substrate of the semiconductor device concerning this invention is characterized by carrying out the laminating of a printed circuit board and the wiring layer formed by resin material. Moreover, the wiring substrate of the semiconductor device concerning this invention is characterized by being the wiring layer which consisted of resin material with flexibility.

[0014] Furthermore, the manufacture approach of the semiconductor device concerning this invention has the process which forms the projection electrode which has the cross-sectional area smaller than this electrode by the ball bonder on the electrode of a semiconductor device, the process which pastes up anisotropy electric conduction adhesives on the field in which the electrode on a wiring substrate and wiring were formed, and the process which pushes a projection electrode against the electrode of a wiring substrate through anisotropy electric conduction adhesives.

[0015] Moreover, the manufacture approach of the semiconductor device concerning this invention The process which forms the layer of the adhesives which do not contain an electric conduction particle in the front face of the semiconductor device which has the projection electrode of the cross section smaller than this electrode on an electrode, It has the process which pushes the semiconductor device in which the layer of the process which forms the layer of anisotropy electric conduction adhesives in the field in which the electrode on a wiring substrate and wiring were formed, and the adhesives which do not contain an electric conduction particle was formed, and the wiring substrate with which the layer of anisotropy electric conduction adhesives was formed, and is pasted up.

[0016]

[Embodiment of the Invention] Hereafter, the gestalt of 1 operation of this invention is explained based on a drawing. In addition, in drawing, the same agreement as the former expresses a thing the same as that of the conventional thing, or considerable.

Gestalt 1. drawing 1 of operation is the sectional view showing the configuration of the semiconductor device by the gestalt 1 of operation of this invention. In drawing, it is the layer of the anisotropy electric conduction adhesives with which the electrode with which 1 was formed in the semiconductor device and 2 was formed on the semiconductor device 1, the wiring substrate with which a projection electrode and 4 consist of a glass substrate in 3, the electrode with which 5 was formed on the wiring substrate 4, and 6 contain a conductive particle, and 7 contains the conductive particle 6.

[0017] In the gestalt of this operation, since the cross section of each projection electrode 3 is formed so that it may become the cross section smaller than the electrode 2 formed on the semiconductor device 1, the distance B between each electrode 2 can take the large spacing A of the projection electrode 3 used for connection with the electrode 5 on a circuit board 4, even when short. Therefore, between the projection electrodes 3, it is mitigated and conductive particle 6 comrades in the layer 7 of anisotropy electric conduction adhesives contacting mutually, or recriminating can secure the good insulation between the projection electrodes 3.

[0018] In addition, the ingredients of the projection electrode 3 on the electrode 2 of a semiconductor device 1 should just be metals, such as gold, copper, nickel, and solder. The formation approach can be performed using the membrane formation technique of metals, such as a photoengraving-process technique, plating, or vacuum evaporationo. The conductive particle 6 turns into plastics particles, such as epoxy whose diameter is about 5 micrometers, from the thing in which metal membranes, such as gold, were formed. The metal particles of nickel or gold may be used for others. Thermoplastic adhesives may be used for it although the epoxy resin of a heat-curing mold was used for the layer 7 of anisotropy electric conduction adhesives as base resin of adhesives.

[0019] Moreover, in the gestalt of this operation, the flow with a good place which connected the semiconductor device 1 which formed the projection electrode 3 of a magnitude the angle of 50 micrometers, for example on the electrode 2 of the semiconductor device in which magnitude and spacing have 60-micrometer angle and 10 micrometers, respectively to the wiring substrate 4 which consisted of glass substrates with the electrode 5 which consists of ingredients of ITO (indium stannic-acid ghost) was able to be obtained. Therefore, according to the gestalt 1 of this operation, in connection with the wiring substrate of a semiconductor device with a detailed electrode spacing, good insulation can be secured and a good flow can be enabled. Moreover, a glass substrate can be wired detailed and can improve the packaging density of a semiconductor device by using a glass substrate as a wiring substrate.

[0020] Gestalt 2. drawing 2 of operation is the sectional view showing the configuration of the semiconductor device by the gestalt 2 of operation of this invention. It is a sectional view. In drawing, it is the layer of the anisotropy electric conduction adhesives with which the electrode with which 1 was formed in the semiconductor device and 2 was formed on the semiconductor device 1, the electrode with which a projection electrode and 40 were formed in the wiring substrate, and 5 was formed for 3 on the wiring substrate 40, and 6 contain a conductive particle, and 7 contains the conductive particle 6. Moreover, as for the conductor layer which a wiring layer and 10 become in 8 and the insulating layer of resin material and 12 become from the metal on a wiring layer 8 in a crevice and 11, and 15, a printed circuit board and 16 are the circuit patterns on a printed circuit board 15.
[0021] Also in the gestalt of this operation, since the cross section of each projection electrode 3 is formed so that it may become the cross section smaller than the electrode 2 formed on the semiconductor device 1, even when the distance between each electrode 2 is short, large spacing of the projection electrode 3 used for connection with the electrode 5 on the wiring substrate 40 can be taken. Therefore, between the projection electrodes 3, it is mitigated and conductive particle 6 comrades in the layer 7 of anisotropy electric conduction adhesives contacting mutually, or recriminating can secure the good insulation between the projection electrodes 3. Furthermore, since the wiring substrate 40 consists of wiring layers 8 which consist of a printed circuit board 15, an insulating layer 11 formed on it, and a conductor layer 12 in the gestalt of this operation as shown in drawing, it becomes lighter than the thing using a glass substrate. Moreover, as for the wiring pitch T of a printed circuit board 15, although about 200 micrometers is a limitation with a present condition technique, wiring pitch T' on a wiring layer 8 can realize detailed wiring of 100 micrometers by using such a wiring substrate 40.
[0022] The wiring substrate 40 is a conductor layer by applying resin, such as epoxy, to the front face of a printed circuit board 15, forming the Bahia hall using a photoengraving-process technique, forming a metal membrane by plating or vacuum evaporationo after forming an insulating layer 11, and carrying out patterning of the metal membrane using a photoengraving-process technique. 12 can be formed on said insulating layer 11. Multilayering of a wiring layer 8 is possible by repeating formation of this insulating layer 11 and a conductor layer 12. The surface irregularity of such a wiring substrate 40 is large, and dispersion produces it in the height of an electrode 5.
[0023] Since the distance between the projection electrode 3 and the electrode 5 of the wiring substrate 40 will differ when irregularity is shown in the front face of the wiring substrate 40, there is a flume problem from which good connection is no longer obtained in no connection places. However, in case the projection electrode 3 is pushed against the electrode 5 of the wiring substrate 40 to this problem, it is solved by pushing in until a crevice 10 produces the electrode 5 of the wiring substrate 40, and it becomes possible to connect certainly all the projection electrodes 3 and electrodes 5 of the wiring substrate 40 through the conductive particle 6. When the semiconductor device 1 which actually has a detailed electrode spacing was connected, the same result as the gestalt 1 of operation was able to be obtained. As mentioned above, according to the gestalt of this operation, the semiconductor device which secured projection inter-electrode good insulation, and attained improvement and lightweight-izing of packaging density is realizable.
[0024] Gestalt 3. drawing 3 of operation is the sectional view showing the configuration of the semiconductor device by the gestalt 3 of operation of this invention. In drawing, it is the layer of the anisotropy electric conduction adhesives with which the electrode with which 1 was formed in the semiconductor device and 2 was formed on the semiconductor device 1, the electrode with which a projection electrode and 8 were formed in the wiring layer, and 5 was formed for 3 on the wiring layer 8, and 6 contain a conductive particle, and 7 contains the conductive particle 6. Moreover, it is the conductor layer which 10 becomes in a crevice and the insulating layer of resin material and 12 become from the metal on a wiring layer 8 in 11. As shown in drawing, with the gestalt of this operation, the wiring layer 8 as shown with the gestalt 2 of operation is used as the wiring substrate itself instead of the wiring substrate 4 which consists of a glass substrate used in the gestalt 1 of operation. The formation approach of a wiring layer 8 uses the same approach as the gestalt 2 of operation. Although the resin of an insulating layer 11 used the epoxy resin with the gestalt 2 of operation, the polyimide which has flexibility more is sufficient as it.
[0025] Moreover, also in the gestalt of this operation, since the cross section of each projection electrode 3 is formed so that it may become the cross section smaller than the electrode 2 formed on the semiconductor device 1, even when the distance between each electrode 2 is short, large spacing of the projection electrode 3 used for connection with the electrode 5 on a wiring layer 8 can be taken. Therefore, between the projection electrodes 3, it is mitigated and conductive particle 6 comrades in the layer 7 of anisotropy electric conduction adhesives contacting mutually, or recriminating can secure the good insulation between the projection electrodes

3.
[0026] Since the distance between the projection electrode 3 and the electrode 5 on a wiring layer 8 will differ when irregularity is shown in the front face of the wiring layer 8 as a wiring substrate, there is a flume problem from which good connection is no longer obtained in no connection places. However, in case the projection electrode 3 is pushed against the electrode 5 of a wiring layer 8 like the case of the gestalt 2 of operation also to this problem, it is solved by pushing in until the electrode 5 of a wiring layer 8 produces a crevice 10, and it becomes possible to connect certainly all the projection electrodes 3 and electrodes 5 on a wiring layer 8 through the conductive particle 6. Furthermore, in the gestalt of this operation, since a wiring layer 8 can absorb enough the thermal stress generated according to the coefficient-of-thermal-expansion difference of a semiconductor device 1 and a wiring layer 8 by having constituted only from a wiring layer 8 using resin material flexible as a wiring substrate, the dependability of the connection over the long period of time of the projection electrode 3 and the electrode 5 on a wiring layer 8 can be improved.
[0027] Gestalt 4. drawing 4 of operation is drawing showing the manufacture approach by the gestalt 4 of operation of this invention. In drawing, it is the layer of the anisotropy electric conduction adhesives with which the electrode with which 1 was formed in the semiconductor device and 2 was formed on the semiconductor device 1, the electrode with which a projection electrode and 4 were formed in the wiring substrate, and 5 was formed for 3 on the wiring substrate 4, and 6 contain a conductive particle, and 7 contains the conductive particle 6. Drawing (a) shows the condition of having formed the projection 13 by the ball bonder on the electrode 2 of a semiconductor device 1. It makes the tip of projection 13 flat and shows the condition of having formed the projection electrode 3 while drawing (b) is monotonous, forces this projection 13 and equalizes the height of projection 13. Drawing (c) shows the condition of having formed the layer 7 of anisotropy electric conduction adhesives on the wiring substrate 4. Furthermore, drawing (d) forces the semiconductor device 1 with the projection electrode 3 on the wiring substrate 4, heats it, and shows the condition that the projection electrode 3 and the electrode 5 of the wiring substrate 4 flowed. Thus, it is effective in the ability to form the projection electrode 3 easily, without passing through complicated processes, such as photoengraving process and plating, by forming the projection electrode 3 using a ball bonder according to the manufacture approach of the semiconductor device by the gestalt of this operation.
[0028] In the gestalt 1 of operation of the gestalt 5. above-mentioned of operation, although a conductive channel may be able to do electrode 2 adjoining comrades through the conductive particle 6 and insulating dependability may deteriorate if the conductive particle 6 exists in the part which has exposed the electrode 2 of a semiconductor device 1 since the electrode 2 of a semiconductor device 1 has the larger cross section than the projection electrode 3, the gestalt of this operation also improves such a trouble. Drawing 5 is the sectional view showing the configuration of the semiconductor device by the gestalt 5 of operation of this invention. In drawing, although the layer of the anisotropy electric conduction adhesives with which the electrode with which 1 was formed in the semiconductor device and 2 was formed on the semiconductor device 1, the electrode with which a projection electrode and 4 were formed in the wiring substrate, and 5 was formed for 3 on the wiring substrate 4, and 6 contain a conductive particle, and 7 contains the conductive particle 6, and 14 use the same adhesives as the layer 7 of anisotropy electric conduction adhesives, the conductive particle 6 is the layer of only the adhesives which are not included.
[0029] Thus, with the gestalt of this operation, the layer of the adhesives of two layers of the layer 7 of the anisotropy electric conduction adhesives containing the conductive particle 6, the layer 7 of these anisotropy electric conduction adhesives, and the layer 14 of only the adhesives which do not contain the conductive particle 6 using the same adhesives is formed between the semiconductor device 1 and the wiring substrate 4. In addition, if the productive efficiency at the time of manufacture is taken into consideration, since it is necessary to harden the adhesives between a semiconductor device 1 and the wiring substrate 4 to coincidence, it is necessary to use the adhesives of the layer 14 of adhesives without the conductive particle 6, and the layer 7 with the conductive particle 6 as the adhesives of the same ingredient.
[0030] Also in the gestalt of this operation, since the cross section of each projection electrode 3 is formed so that it may become the cross section smaller than the electrode 2 formed on the semiconductor device 1, the distance B between each [electrode 2] can take the large spacing A of projection electrode 3 comrades used for connection with the electrode 5 on the wiring substrate 4, even when short. Therefore, in the layer 7 of anisotropy electric conduction adhesives, between each projection electrode 3, it is mitigated and conductive particle 6 comrades contacting mutually, or recriminating can secure the good insulation between the projection electrodes 3. Furthermore, since it prevents certainly that a conductive channel is made through the conductive

particle 6 between electrode 2 comrades which adjoin by constituting the layer 14 of only the adhesives which do not contain the conductive particle 6 in the field by the side of the wiring substrate 4 of a semiconductor device 1 as shown in drawing 5 , it can prevent that insulating dependability deteriorates between the electrodes 2 formed in the field by the side of the wiring substrate 4 of a semiconductor device 1.

[0031] Gestalt 6. drawing 6 of operation is the sectional view showing the manufacture approach by the gestalt 6 of operation of this invention. In drawing, although the layer of the anisotropy electric conduction adhesives with which the electrode with which 1 was formed in the semiconductor device and 2 was formed on the semiconductor device 1, the electrode with which a projection electrode and 4 were formed in the wiring substrate, and 5 was formed for 3 on the wiring substrate 4, and 6 contain a conductive particle, and 7 contains the conductive particle 6, and 14 use the same adhesives as the layer 7 of anisotropy electric conduction adhesives, the conductive particle 6 is the layer of only the adhesives which are not included. Drawing 6 (a) shows the condition of having formed the layer 14 of only adhesives without the conductive particle 6 in the front face of the semiconductor device 1 in which the projection electrode 3 was formed. Drawing 6 (b) shows the condition of having formed the layer 7 of anisotropy electric conduction adhesives on the wiring substrate 4. The condition heated and hardened the layer 14 of only adhesives and the layer 7 of anisotropy electric-conduction adhesives without the conductive particle 6 is shown at the same time drawing 6 (c) forces and heats the semiconductor device 1 in_which the layer 14 of only the adhesives which do not have the conductive particle 6 to the wiring substrate 4 in_which the layer 7 of anisotropy electric-conduction adhesives was formed was formed and it takes a flow with the projection electrode 3 of a semiconductor device 1, and the electrode 5 on the wiring substrate 4.

[0032] Thus, by forming the layer 14 of only adhesives without the conductive particle 6 in the front face of a semiconductor device 1 beforehand It becomes possible to separate completely the layer 7 of anisotropy electric conduction adhesives with the conductive particle 6, and the layer 14 of only adhesives without the conductive particle 6. In case a semiconductor device 1 is forced and heated to the wiring substrate 4 and adhesives are hardened, adhesives can become soft and flow and it can prevent completely that the conductive particle 6 exists between the electrodes 2 on a semiconductor device 1. Therefore, the semiconductor device which prevents that a conductive channel is made through the conductive particle 6 between electrode 2 comrades adjoined on the manufacture approach ****** of the semiconductor device by the gestalt of this operation and a semiconductor device 1, and can prevent that insulating dependability deteriorates between the electrodes 2 formed in the field by the side of the wiring substrate 4 of a semiconductor device 1 is realizable.

[0033]

[Effect of the Invention] The semiconductor device which has the projection electrode of the cross section smaller than this electrode on an electrode according to this invention, Since it had the layer of the anisotropy electric conduction adhesives which it is formed [adhesives] between the wiring substrate which has a projection electrode and the electrode arranged in the location which counters, and a semiconductor device and a wiring substrate, and make it flow through a projection electrode and the electrode on said wiring substrate which counters this In connection with the wiring substrate of a semiconductor device with a detailed electrode spacing, it is effective in the ability to offer the semiconductor device which can enlarge projection inter-electrode distance, can secure good insulation and can enable a good flow.

[0034] Moreover, the semiconductor device which has the projection electrode of the cross section smaller than this electrode on an electrode according to this invention, It is the semiconductor device equipped with the two or more layers layer of adhesives formed between the wiring substrate which has a projection electrode and the electrode arranged in the location which counters, and a semiconductor device and a wiring substrate. By being in a layer [of the adhesives which the two or more layers layer of adhesives has in a semiconductor device side, and do not contain an electric conduction particle], and wiring substrate side, and constituting from a layer of the anisotropy electric conduction adhesives which make it flow through a projection electrode and the electrode on the wiring substrate which counters this Since it can prevent certainly that a conductive channel is made through a conductive particle among the electrodes which projection inter-electrode good insulation is secured to, and a semiconductor device adjoins, it is effective in a very good insulating semiconductor device being realizable.

[0035] Moreover, according to this invention, since that wiring substrate uses the glass substrate in which detailed wiring is possible, it is effective in the semiconductor device which can secure good insulation and can aim at improvement in packaging density being realizable. Moreover, since that wiring substrate carried out the laminating of a printed circuit board and the wiring layer formed by resin material according to this invention, it is effective in the semiconductor device which secured good insulation and attained improvement and lightweight-izing of packaging density being realizable. Moreover, according to this invention, since that wiring substrate used

the wiring layer which consisted of resin material with flexibility, it is effective in the semiconductor device which secures good insulation and can aim at improvement in the dependability of connection over a long period of time being realizable.

[0036] Moreover, since it has the process which forms the projection electrode which has the cross-sectional area smaller than this electrode by the ball bonder on the electrode of a semiconductor device according to this invention, formation of a projection electrode makes complicated processes, such as photoengraving process and plating, unnecessary, and is effective in the ability to offer the manufacture approach of a semiconductor device with sufficient productive efficiency.

[0037] Moreover, the process which forms the layer of the adhesives which do not contain an electric conduction particle in the front face of the semiconductor device which has the projection electrode of the cross section smaller than this electrode on an electrode according to this invention, The process which forms the layer of anisotropy electric conduction adhesives in the field in which the electrode on a wiring substrate and wiring were formed, Since it has the process which pushes the semiconductor device in which the layer of the adhesives which do not contain an electric conduction particle was formed, and the wiring substrate with which the layer of anisotropy electric conduction adhesives was formed, and is pasted up It can prevent certainly that a conductive channel is made through a conductive particle among the electrodes which a semiconductor device adjoins, and is effective in the ability to offer the manufacture approach of a very good insulating semiconductor device.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view showing the configuration of the semiconductor device by the gestalt 1 of operation of this invention.

[Drawing 2] It is the sectional view showing the configuration of the semiconductor device by the gestalt 2 of operation of this invention.

[Drawing 3] It is the sectional view showing the configuration of the semiconductor device by the gestalt 3 of operation of this invention.

[Drawing 4] It is drawing for explaining the manufacture approach of the semiconductor device by the gestalt 4 of operation of this invention.

[Drawing 5] It is the sectional view showing the configuration of the semiconductor device by the gestalt 5 of operation of this invention.

[Drawing 6] It is drawing for explaining the manufacture approach of the semiconductor device by the gestalt 6 of operation of this invention.

[Drawing 7] It is the sectional view showing the configuration of the conventional semiconductor device.

[Drawing 8] It is the sectional view showing the configuration of the conventional semiconductor device.

[Drawing 9] It is the sectional view showing the configuration of the conventional semiconductor device using anisotropy electric conduction adhesives.

[Description of Notations]

1 Semiconductor Device 2 Electrode on Semiconductor Device 3 Projection Electrode
4 Wiring Substrate 5 Electrode on Wiring Substrate 6 Conductive Particle
7 Layer of Anisotropy Electric Conduction Adhesives 8 Wiring Layer 9 Electric Conduction Lead
10 Crevice of Wiring Substrate 11 Insulating Layer 12 Conductor Layer

13 Projection 14 Layer of Only Adhesives 15 Printed Circuit Board
16 Circuit Pattern 21 Electroconductive Glue 22 Encapsulant
23 Solder

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（A）　(11)特許出願公開番号
特開平10－125725
(43)公開日　平成10年(1998)５月15日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｈ０１Ｌ　21/60	３１１	Ｈ０１Ｌ　21/60	３１１Ｓ

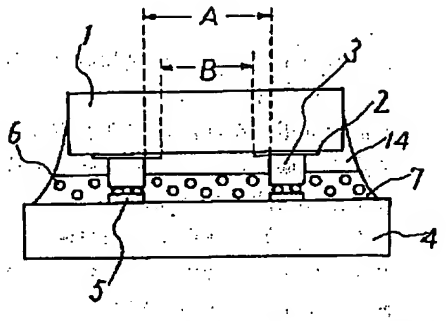
審査請求　未請求　請求項の数７　ＯＬ　（全８頁）

(21)出願番号　特願平8－276053
(22)出願日　平成８年(1996)10月18日

(71)出願人　000006013
三菱電機株式会社
東京都千代田区丸の内二丁目２番３号
(72)発明者　濱口　恒夫
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(72)発明者　鶴田　明三
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(72)発明者　利田　賢二
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(74)代理人　弁理士　宮田　金雄　（外３名）
最終頁に続く

(54)【発明の名称】　半導体装置およびその製造方法

(57)【要約】
【課題】　半導体素子の突起電極間に介在する異方性導電接着剤の導電粒子同士が擦りあって突起電極間の絶縁性が劣化したり、半導体素子の隣接電極間において導電性粒子を介して導通チャンネルができ、電極間の絶縁性が劣化する。
【解決手段】　電極２上に該電極より小さな断面積の突起電極３を有する半導体素子１と、突起電極３と対向する位置に配設された電極５を有する配線基板４と、半導体素子１と配線基板４との間に形成された複数層の接着剤の層とを備えた半導体装置であって、複数層の接着剤の層は半導体素子１の側にあって導電粒子６を含まない接着剤のみの層１４と配線基板４の側にあって突起電極３とこれに対向する配線基板上の電極５とを導通させる異方性導電接着剤の層７とで構成した。



1：半導体素子　2：半導体素子上の電極　3：突起電極
4：配線基板　5：配線基板上の電極　6：導電性粒子
7：異方性導電接着剤の層
14：接着剤のみの層

1

【特許請求の範囲】

【請求項１】　電極上に該電極より小さな断面積の突起電極を有する半導体素子と、
前記突起電極と対向する位置に配設された電極を有する配線基板と、
前記半導体素子と前記配線基板との間に形成され、前記突起電極とこれに対向する前記配線基板上の電極とを導通させる異方性導電接着剤の層とを備えたことを特徴とする半導体装置。

【請求項２】　電極上に該電極より小さな断面積の突起電極を有する半導体素子と、
前記突起電極と対向する位置に配設された電極を有する配線基板と、
前記半導体素子と前記配線基板との間に形成された複数層の接着剤の層とを備えた半導体装置であって、
前記複数層の接着剤の層は、前記半導体素子の側にあって導電粒子を含まない接着剤の層と前記配線基板の側にあって前記突起電極とこれに対向する前記配線基板上の電極とを導通させる異方性導電接着剤の層とで構成されていることを特徴とする半導体装置。

【請求項３】　配線基板は、ガラス基板であることを特徴とする請求項１または２記載の半導体装置。

【請求項４】　配線基板は、プリント基板と樹脂材で形成された配線層とを積層したものであることを特徴とする請求項１または２記載の半導体装置。

【請求項５】　配線基板は、可とう性を有した樹脂材で構成された配線層であることを特徴とする請求項１または２記載の半導体装置。

【請求項６】　半導体素子の電極上に該電極より小さな断面積を有する突起電極をボールボンダで形成する工程と、
異方性導電接着剤を配線基板上の電極および配線が形成された面に接着する工程と、
前記突起電極を前記異方性導電接着剤を介して前記配線基板の電極に押し付ける工程とを有したことを特徴とする半導体装置の製造方法。

【請求項７】　電極上に該電極より小さな断面積の突起電極を有する半導体素子の表面に導電粒子を含まない接着剤の層を形成する工程と、
異方性導電接着剤の層を配線基板上の電極および配線が形成された面に形成する工程と、
前記導電粒子を含まない接着剤の層が形成された半導体素子と異方性導電接着剤の層が形成された配線基板とを押し付けて接着する工程とを有したことを特徴とする半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体素子と配線基板の電極同士を異方性導電接着剤で接続することによって得られる半導体装置およびその製造方法に関するものである。

2

【０００２】

【従来の技術】電子機器をより小型化するために、パッケージされた半導体素子を配線基板にはんだ付けする方法から、パッケージしないで裸のまま半導体素子を配線基板に実装する方法に変わってきた。半導体素子を裸のままで配線基板に実装する方法として、半導体素子の裏面を配線基板に導電性接着剤で接着し、半導体素子の電極と配線基板の電極とをワイヤで接続する方法がある。この方法は半導体素子と配線基板の電極とを一本一本ワイヤで接続するため、多数の電極を接続するのに時間がかかる。また、接続される配線基板の電極を半導体素子の周辺に配置するため、実装面積が半導体素子の面積よりも大きくとる必要がある。そこで、半導体素子とほぼ同じ面積で実装する方法として、半導体素子を裏返して、配線基板電極に直接接続するフリップチップ接続方法が開発された。

【０００３】その方法として、（１）導電性接着剤を用いて接続する方法（例えば、日刊工業新聞社発行、表面実装技術、９月号１９９４年、４８ページ）と（２）はんだを用いて接続する方法（例えば、工業調査会、１９８６年６月１日発行、サーフェイス・マウント・テクノロジー、１７２ページ）がある。以下、図面を参照しながら説明する。図７は、導電性接着剤を用いて接続した従来の半導体装置の構成を示す断面図である。図において、１はパッケージしていない裸の半導体素子、２は半導体素子１の上に形成された電極、３はこの半導体素子上の電極２の上に形成された突起電極、４は配線基板、５は配線基板４上に形成された電極、２１は導電性接着剤、２２は封止剤を示す。

【０００４】このような構造を有した従来の半導体装置の製造方法について説明する。まず、めっきを用いて、半導体素子１の電極２上に突起電極３を形成する。次に、平面板に均一膜厚に形成された導電性接着剤層（図示せず）に、この突起電極３を押し付け、導電性接着剤２１を突起電極３に転写する。次に、半導体素子１と配線基板４を向かい合わせ、半導体素子１の突起電極３と配線基板４上の電極５との位置合わせた後に、半導体素子１を配線基板４に押し付け、突起電極３と配線基板４上の電極５とを導電性接着剤２１を介して接触させる。次に、約１５０℃の条件で数時間加熱して導電性接着剤２１を硬化させた後に、外部から湿気等の侵入を防ぐための封止剤２２を半導体素子１と配線基板４の間に注入し、加熱硬化させることにより図７に示した半導体装置を得ることができる。

【０００５】図８は、はんだを用いて接続する場合の従来の半導体装置の構成を示す断面図である。図において、１は半導体素子、２は半導体素子１の上に形成された電極、３はこの半導体素子上の電極２上に形成された突起電極、４は配線基板、５は配線基板４の上に形成さ

れた電極、２２は封止剤、２３ははんだを示す。このような構造を有した従来の半導体装置の製造方法について説明する。まず、半導体素子１の上に形成された電極の２上に、蒸着等でＣｒ、Ｃｕの膜を形成した後、レジストをパターニングして、めっきまたは蒸着で、Ｐｂ－Ｓｎのはんだの突起電極３を形成する。次に、あらかじめ共晶はんだ２３を供給してある配線基板４上の電極５と位置合わせを行い、半導体素子１を加熱してはんだ２３を溶融させて、突起電極３と電極５を接合し、半導体素子１と配線基板４の間に封止剤２２を注入し、加熱硬化させることにより、図８に示した半導体装置を得ることができる。

【０００６】図９は、例えば、特公昭６２－６６５２号公報に記載された異方性導電接着剤によって半導体素子と配線基板とを接続する従来の半導体装置の構成を示す断面図である。図において、１は半導体素子、２は半導体素子１の上に形成された電極、３はこの半導体素子上の電極２上に形成された突起電極、４は配線基板、７は異方性導電接着剤の層、９は配線基板４上の導電リード線を示す。なお、異方性導電接着剤とは、接着剤中に金属粒子、プラスチックボールの表面に金属をめきした粒子などを分散したもので、圧力が加えられると接着剤が排除され、電気的な導通が得られるものである。

【０００７】配線基板４上の導電リード線９上に異方性導電接着剤の層７を形成し、突起電極３を有した半導体素子１を押し付けると、突起電極３の下の部分の異方性導電接着剤の層７は圧力が加えられた方向に導通する。これにより、突起電極３と導電リード９は導通する。同時に、半導体素子１は配線基板４に異方性導電接着剤の層７の接着作用によって固着され、外部からの湿気やほこりの侵入を防止することができる。また、半導体素子１の下面は異方性導電接着剤の層７によって全面的に配線基板４に接着しているので接着面積が広くなり接合強度も強くなる。

【０００８】

【発明が解決しようとする課題】図７、図８に示した従来の半導体装置には以下の問題点があった。

（１）半導体素子を接続のため、配線基板電極に押し当てた時に、導電性接着剤またははんだの接着剤が横に広がり、隣接の電極と接触し、ショートが発生し、微細電極間距離の半導体素子の接続ができない。

（２）半導体素子の突起電極と配線基板の電極を導電性接着剤またははんだで接続してから、信頼性を高めるために半導体素子と配線基板間に封止剤を注入するため、プロセスが多く生産性に欠ける。

【０００９】図９に示した従来技術はこれらの問題点を一応解決してはいるが、突起電極間Ａには導電性接着剤の導電性の粒子は存在し、電極間隔Ａが狭くなる微細電極を有する半導体素子においては、突起電極間の導電性粒子同士が擦りあって、突起電極間の絶縁抵抗が劣化したり、半導体素子の表面での電極間に導電粒子による導通チャンネルができて電極間の絶縁性が劣化するという問題点があった。

【００１０】本発明は、電極間隔の狭い微細電極を有する半導体素子においても、電極間に介在する導電性接着剤の導電粒子に起因する絶縁性の劣化を防止し、さらに配線基板との良好なる接続を生産性良く実現する半導体装置およびその製造方法を提供することを目的としている。

【００１１】

【課題を解決するための手段】この発明に係る半導体装置は、電極上に該電極より小さな断面積の突起電極を有する半導体素子と、突起電極と対向する位置に配設された電極を有する配線基板と、半導体素子と配線基板との間に形成され、突起電極とこれに対向する前記配線基板上の電極とを導通させる異方性導電接着剤の層とを備えたものである。

【００１２】また、この発明に係る半導体装置は、電極上に該電極より小さな断面積の突起電極を有する半導体素子と、突起電極と対向する位置に配設された電極を有する配線基板と、半導体素子と配線基板との間に形成された複数層の接着剤の層とを備えた半導体装置であって、複数層の接着剤の層は、半導体素子の側にあって導電粒子を含まない接着剤の層と配線基板の側にあって突起電極とこれに対向する配線基板上の電極とを導通させる異方性導電接着剤の層とで構成されたものである。

【００１３】また、この発明に係る半導体装置の配線基板は、ガラス基板であることを特徴とするものである。また、この発明に係る半導体装置の配線基板は、プリント基板と樹脂材で形成された配線層とを積層したことを特徴とするものである。また、この発明に係る半導体装置の配線基板は、可とう性を有した樹脂材で構成された配線層であることを特徴とするものである。

【００１４】さらに、この発明に係る半導体装置の製造方法は、半導体素子の電極上に該電極より小さな断面積を有する突起電極をボールボンダで形成する工程と、異方性導電接着剤を配線基板上の電極および配線が形成された面に接着する工程と、突起電極を異方性導電接着剤を介して配線基板の電極に押し付ける工程とを有したものである。

【００１５】また、この発明に係る半導体装置の製造方法は、電極上に該電極より小さな断面積の突起電極を有する半導体素子の表面に導電粒子を含まない接着剤の層を形成する工程と、異方性導電接着剤の層を配線基板上の電極および配線が形成された面に形成する工程と、導電粒子を含まない接着剤の層が形成された半導体素子と異方性導電接着剤の層が形成された配線基板とを押し付けて接着する工程とを有したものである。

【００１６】

【発明の実施の形態】以下、本発明の一実施の形態を図

5

面に基づいて説明する。尚、図において従来と同一符合は従来のものと同一あるいは相当のものを表す。

実施の形態１．図１は、本発明の実施の形態１による半導体装置の構成を示す断面図である。図において、１は半導体素子、２は半導体素子１上に形成された電極、３は突起電極、４は例えばガラス基板からなる配線基板、５は配線基板４上に形成された電極、６は導電性粒子、７は導電性粒子６を含む異方性導電接着剤の層である。

【００１７】本実施の形態においては、各突起電極３の断面積は、半導体素子１上に形成された電極２より小さい断面積となるように形成されているので、各電極２の間の距離Ｂが短い場合でも配線基盤４上の電極５との接続に用いられる突起電極３の間隔Ａは大きくとれる。そのため、突起電極３の間において異方性導電接着剤の層７中の導電性粒子６同士が互いに接触したり、擦りあうことは軽減され、突起電極３間の良好な絶縁性を確保することができる。

【００１８】尚、半導体素子１の電極２上の突起電極３の材料は金、銅、ニッケル、はんだ等の金属であればよい。その形成方法は写真製版技術とめっきまたは蒸着等の金属の成膜技術を用いて行うことができる。導電性粒子６は直径が５μｍ程度のエポキシ等のプラスチック粒子に金等の金属膜を形成したものからなる。他に、ニッケルまたは金の金属粒子を用いてもよい。異方性導電接着剤の層７は、接着剤の主剤として熱硬化型のエポキシ樹脂を用いたが、熱可塑性の接着剤を用いてもよい。

【００１９】また、本実施の形態においては、例えば、大きさと間隔がそれぞれ６０μｍ角と１０μｍをもつ半導体素子の電極２の上に、大きさ５０μｍ角の突起電極３を形成した半導体素子１をＩＴＯ（インジウム・スズ酸化物）の材料で構成される電極５を有したガラス基板で構成された配線基板４に接続したところ良好な導通を得ることができた。従って、本実施の形態１によれば、微細な電極間隔を有した半導体素子の配線基板への接続において良好な絶縁性を確保し、かつ良好な導通を可能にすることができる。また、ガラス基板は微細配線が可能であり、配線基板としてガラス基板を用いることにより半導体素子の実装密度を向上することができる。

【００２０】実施の形態２．図２は、本発明の実施の形態２による半導体装置の構成を示す断面図である。断面図である。図において、１は半導体素子、２は半導体素子１上に形成された電極、３は突起電極、４０は配線基板、５は配線基板４０上に形成された電極、６は導電性粒子、７は導電性粒子６を含む異方性導電接着剤の層である。また、８は配線層、１０は凹部、１１は樹脂材の絶縁層、１２は配線層８上の金属からなる導体層、１５はプリント基板、１６はプリント基板１５上の配線パターンである。

【００２１】本実施の形態においても、各突起電極３の断面積は、半導体素子１上に形成された電極２より小さい断面積となるように形成されているので、各電極２の間の距離が短い場合でも配線基板４０上の電極５との接続に用いられる突起電極３の間隔は大きくとれる。そのため、突起電極３の間において異方性導電接着剤の層７中の導電性粒子６同士が互いに接触したり、擦りあうことは軽減され、突起電極３間の良好な絶縁性を確保することができる。さらに、図に示すように本実施の形態においては、配線基板４０はプリント基板１５とその上に形成された絶縁層１１と導体層１２からなる配線層８で構成されているので、ガラス基板を用いたものより軽くなる。また、プリント基板１５の配線ピッチＴは現状技術では２００μｍ程度が限界であるが、このような配線基板４０を用いることによって、配線層８上での配線ピッチＴ′は１００μｍという微細配線を実現できる。

【００２２】配線基板４０はプリント基板１５の表面にエポキシ等の樹脂を塗布し、写真製版技術を用いてバイアホールを形成して絶縁層１１を形成後、めっきまたは蒸着等で金属膜を成膜し、写真製版技術を用いて、金属膜をパターニングすることによって、導体層１２を前記絶縁層１１上に形成することができる。この絶縁層１１と導体層１２の形成を繰返すことにより配線層８の多層化が可能である。このような配線基板４０は表面の凹凸が大きく、電極５の高さにばらつきが生じる。

【００２３】配線基板４０の表面に凹凸があると、突起電極３と配線基板４０の電極５との間の距離が異なることになるので、すべての接続箇所において良好な接続が得られなくなるとい問題がある。しかし、この問題に対しては突起電極３を配線基板４０の電極５に押し付ける際に、配線基板４０の電極５を凹部１０が生ずるまで押込むことによって解決され、すべての突起電極３と配線基板４０の電極５とは導電性粒子６を介して確実に接続することが可能になる。実際に、微細な電極間隔を有する半導体素子１を接続したところ、実施の形態１と同様な結果を得ることができた。以上のように、本実施の形態によれば、突起電極間の良好な絶縁性を確保し、かつ、実装密度の向上と軽量化を図った半導体装置を実現できる。

【００２４】実施の形態３．図３は、本発明の実施の形態３による半導体装置の構成を示す断面図である。図において、１は半導体素子、２は半導体素子１上に形成された電極、３は突起電極、８は配線層、５は配線層８上に形成された電極、６は導電性粒子、７は導電性粒子６を含む異方性導電接着剤の層である。また、１０は凹部、１１は樹脂材の絶縁層、１２は配線層８上の金属からなる導体層である。図に示すように、本実施の形態では、実施の形態１において用いたガラス基板からなる配線基板４の代わりに、実施の形態２で示したような配線層８を配線基板そのものとして用いたものである。配線層８の形成方法は実施の形態２と同様の方法を用いる。絶縁層１１の樹脂は実施の形態２ではエポキシ樹脂を用

6

いたが、より可とう性のあるポリイミドでもよい。

【００２５】また、本実施の形態においても、各突起電極３の断面積は、半導体素子１上に形成された電極２より小さい断面積となるように形成されているので、各電極２の間の距離が短い場合でも配線層８上の電極５との接続に用いられる突起電極３の間隔は大きくとれる。そのため、突起電極３の間において異方性導電接着剤の層７中の導電性粒子６同士が互いに接触したり、擦りあうことは軽減され、突起電極３間の良好な絶縁性を確保することができる。

【００２６】配線基板としての配線層８の表面に凹凸があると、突起電極３と配線層８上の電極５との間の距離が異なることになるので、すべての接続箇所において良好な接続が得られなくなるとい問題がある。しかし、この問題に対しても実施の形態２の場合と同様に、突起電極３を配線層８の電極５に押し付ける際に、配線層８の電極５が凹部１０を生ずるまで押込むことによって解決され、すべての突起電極３と配線層８上の電極５とは導電性粒子６を介して確実に接続することが可能になる。さらに、本実施の形態においては、配線基板としてフレキシブルな樹脂材を用いた配線層８のみで構成したことにより、配線層８は半導体素子１と配線層８との熱膨張係数差により発生する熱応力を十分吸収できるので、突起電極３と配線層８上の電極５との長期間にわたる接続の信頼性を向上することができる。

【００２７】実施の形態４．図４は、本発明の実施の形態４による製造方法を示す図である。図において、１は半導体素子、２は半導体素子１上に形成された電極、３は突起電極、４は配線基板、５は配線基板４上に形成された電極、６は導電性粒子、７は導電性粒子６を含む異方性導電接着剤の層である。図（ａ）は、半導体素子１の電極２上にボールボンダで突起１３を形成した状態を示す。図（ｂ）は、この突起１３を平板で押し付け、突起１３の高さを均等にすると共に、突起１３の先端を平坦にし、突起電極３を形成した状態を示す。図（ｃ）は、配線基板４上に異方性導電接着剤の層７を形成した状態を示す。さらに、図（ｄ）は突起電極３をもつ半導体素子１を配線基板４に押し付けて加熱し、突起電極３と配線基板４の電極５が導通した状態を示す。このように本実施の形態による半導体装置の製造方法によれば、ボールボンダを用いて突起電極３を形成することにより、写真製版やめっきなどの煩雑な工程を経ることなく、容易に突起電極３を形成できるという効果がある。

【００２８】実施の形態５．前述の実施の形態１においては、半導体素子１の電極２は突起電極３より大きい断面積を有しているため、半導体素子１の電極２の露出している部分に導電性粒子６が存在すると、隣接する電極２同士が導電性粒子６を介して導通チャネルができ、絶縁信頼性が劣化する場合があるが、本実施の形態はこのような問題点をも改善するものである。図５は、本発明の実施の形態５による半導体装置の構成を示す断面図である。図において、１は半導体素子、２は半導体素子１上に形成された電極、３は突起電極、４は配線基板、５は配線基板４上に形成された電極、６は導電性粒子、７は導電性粒子６を含む異方性導電接着剤の層、１４は異方性導電接着剤の層７と同一の接着剤を用いているが導電性粒子６は含まない接着剤のみの層である。

【００２９】このように、本実施の形態では、半導体素子１と配線基板４間には導電性粒子６を含む異方性導電接着剤の層７とこの異方性導電接着剤の層７と同じ接着剤を用い導電性粒子６を含まない接着剤のみの層１４の２つの層の接着剤の層が形成されている。尚、製造時の生産効率を考慮すると、半導体素子１と配線基板４間の接着剤を同時に硬化する必要があるため、導電性粒子６のない接着剤の層１４と導電性粒子６のある層７の接着剤は同一材料の接着剤にする必要がある。

【００３０】本実施の形態においても、各突起電極３の断面積は、半導体素子１上に形成された電極２より小さい断面積となるように形成されているので、各電極２同士の間の距離Ｂが短い場合でも配線基板４上の電極５との接続に用いられる突起電極３同士の間隔Ａは大きくとれる。そのため、異方性導電接着剤の層７中では、各突起電極３の間において導電性粒子６同士が互いに接触したり、擦りあうことは軽減され、突起電極３間の良好な絶縁性を確保することができる。さらに、図５に示すように半導体素子１の配線基板４側の面には導電性粒子６を含まない接着剤のみの層１４を構成することにより、隣接する電極２同士の間に導電性粒子６を介して導通チャネルができるのを確実に防止するので、半導体素子１の配線基板４側の面に形成された電極２間で絶縁信頼性が劣化するのを防止できる。

【００３１】実施の形態６．図６は、本発明の実施の形態６による製造方法を示す断面図である。図において、１は半導体素子、２は半導体素子１上に形成された電極、３は突起電極、４は配線基板、５は配線基板４上に形成された電極、６は導電性粒子、７は導電性粒子６を含む異方性導電接着剤の層、１４は異方性導電接着剤の層７と同一の接着剤を用いているが導電性粒子６は含まない接着剤のみの層である。図６（ａ）は、突起電極３を形成した半導体素子１の表面に導電性粒子６のない接着剤のみの層１４を形成した状態を示す。図６（ｂ）は、配線基板４の上に異方性導電接着剤の層７を形成した状態を示す。図６（ｃ）は、異方性導電接着剤の層７を形成した配線基板４に対して導電性粒子６のない接着剤のみの層１４を形成した半導体素子１を押し付けて加熱し、半導体素子１の突起電極３と配線基板４上の電極５との導通をとると同時に、導電性粒子６のない接着剤のみの層１４と異方性導電接着剤の層７を加熱して硬化した状態を示す。

【００３２】このように、あらかじめ半導体素子１の表

面に導電性粒子６のない接着剤のみの層１４を形成しておくことにより、導電性粒子６のある異方性導電接着剤の層７と導電性粒子６のない接着剤のみの層１４を完全に分離することが可能となり、配線基板４に半導体素子１を押し付け加熱して接着剤を硬化する際に、接着剤が軟化して流動し、導電性粒子６が半導体素子１上の電極２の間に存在することを完全に防止することができる。従って、本実施の形態による半導体装置の製造方法よれば、半導体素子１上の隣接する電極２同士の間に導電性粒子６を介して導通チャネルができるのを防止し、半導体素子１の配線基板４側の面に形成された電極２の間で絶縁信頼性が劣化するのを防止できる半導体装置を実現することができる。

【００３３】

【発明の効果】この発明によれば、電極上に該電極より小さな断面積の突起電極を有する半導体素子と、突起電極と対向する位置に配設された電極を有する配線基板と、半導体素子と配線基板との間に形成され、突起電極とこれに対向する前記配線基板上の電極とを導通させる異方性導電接着剤の層とを備えたので、微細な電極間隔を有した半導体素子の配線基板への接続において、突起電極間の距離を大きくすることができ、良好な絶縁性を確保し、かつ良好な導通を可能にすることができる半導体装置を提供できるという効果がある。

【００３４】また、この発明によれば、電極上に該電極より小さな断面積の突起電極を有する半導体素子と、突起電極と対向する位置に配設された電極を有する配線基板と、半導体素子と配線基板との間に形成された複数層の接着剤の層とを備えた半導体装置であって、複数層の接着剤の層は、半導体素子の側にあって導電粒子を含まない接着剤の層と配線基板の側にあって突起電極とこれに対向する配線基板上の電極とを導通させる異方性導電接着剤の層とで構成することにより、突起電極間の良好な絶縁性を確保し、かつ、半導体素子の隣接する電極同士の間に導電性粒子を介して導通チャネルができるのを確実に防止することができるので、絶縁性の非常に良好な半導体装置を実現できるという効果がある。

【００３５】また、この発明によれば、その配線基板は微細な配線が可能なガラス基板を用いるので、良好な絶縁性を確保し、かつ、実装密度の向上を図ることのできる半導体装置を実現できるという効果がある。また、この発明によれば、その配線基板はプリント基板と樹脂材で形成された配線層とを積層したので、良好な絶縁性を確保し、かつ、実装密度の向上と軽量化を図った半導体装置を実現できるという効果がある。また、この発明によれば、その配線基板は可とう性を有した樹脂材で構成された配線層を用いたので、良好な絶縁性を確保し、かつ、長期間にわたる接続の信頼性の向上が図れる半導体装置を実現することができるという効果がある。

【００３６】また、この発明によれば、半導体素子の電極上に該電極より小さな断面積を有する突起電極をボールボンダで形成する工程を有しているので、突起電極の形成は写真製版やめっきなどの複雑な工程を不要とし、生産効率のよい半導体装置の製造方法を提供できるという効果がある。

【００３７】また、この発明によれば、電極上に該電極より小さな断面積の突起電極を有する半導体素子の表面に導電粒子を含まない接着剤の層を形成する工程と、異方性導電接着剤の層を配線基板上の電極および配線が形成された面に形成する工程と、導電粒子を含まない接着剤の層が形成された半導体素子と異方性導電接着剤の層が形成された配線基板とを押し付けて接着する工程とを有しているので、半導体素子の隣接する電極同士の間に導電性粒子を介して導通チャネルができるのを確実に防止することができ、絶縁性の非常に良好な半導体装置の製造方法を提供できるという効果がある。

【図面の簡単な説明】

【図１】本発明の実施の形態１による半導体装置の構成を示す断面図である。

【図２】本発明の実施の形態２による半導体装置の構成を示す断面図である。

【図３】本発明の実施の形態３による半導体装置の構成を示す断面図である。

【図４】本発明の実施の形態４による半導体装置の製造方法を説明するための図である。

【図５】本発明の実施の形態５による半導体装置の構成を示す断面図である。

【図６】本発明の実施の形態６による半導体装置の製造方法を説明するための図である。

【図７】従来の半導体装置の構成を示す断面図である。

【図８】従来の半導体装置の構成を示す断面図である。

【図９】異方性導電接着剤を用いた従来の半導体装置の構成を示す断面図である。

【符号の説明】

１　半導体素子　２　半導体素子上の電極　３　突起電極

４　配線基板　５　配線基板上の電極　６　導電性粒子

７　異方性導電接着剤の層　８　配線層　９　導電リード

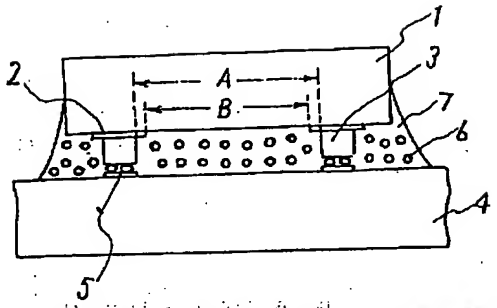
１０　配線基板の凹部　１１　絶縁層　１２　導体層

１３　突起　１４　接着剤のみの層　１５　プリント基板

１６　配線パターン　２１　導電性接着剤　２２　封止剤

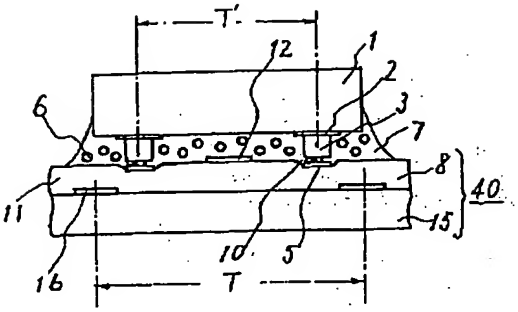
２３　はんだ

【図１】

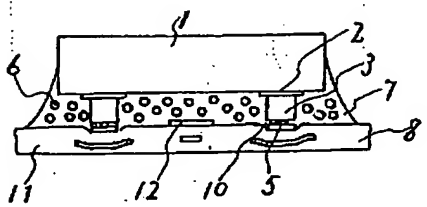


1：半導体素子　2：半導体素子上の電極　3：突起電極
4：配線基板　5：配線基板上の電極　6：導電性粒子
7：異方性導電接着剤の層

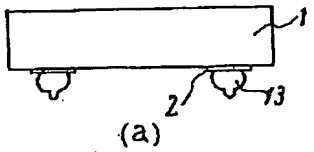
【図２】



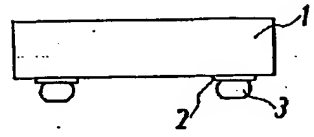
【図３】



【図４】

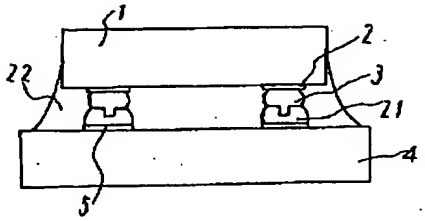


(a)

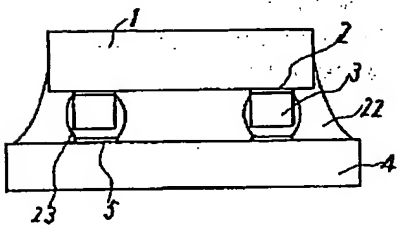


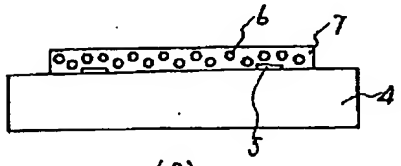
(b)

【図７】

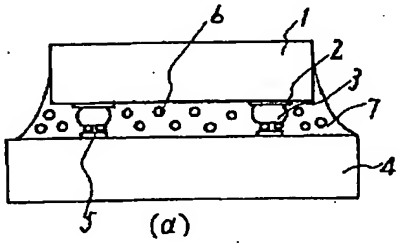


【図８】



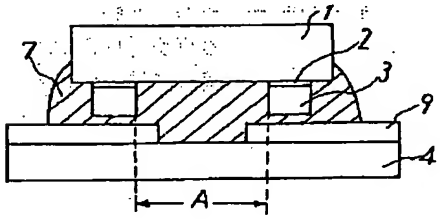


(c)

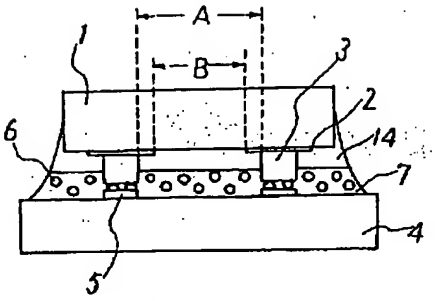


(d)

【図９】

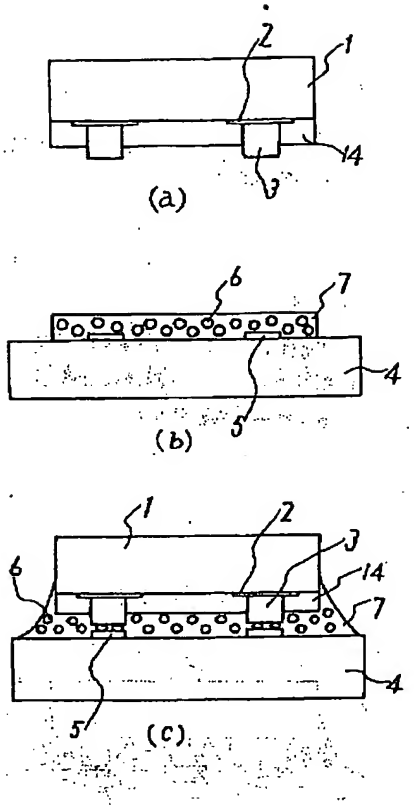


【図５】



1：半導体素子　2：半導体素子上の電極　3：突起電極
4：配線基板　5：配線基板上の電極　6：導電性粒子
7：異方性導電接着剤の層
14：接着剤のみの層

【図６】



フロントページの続き

(72)発明者　石崎　光範
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内

(72)発明者　北村　洋一
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内

(72)発明者　長嶺　高宏
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内